REMARKS/ARGUMENTS

Claims 1-14 are pending in this application, of which claims 1, 6 and 8 are independent. No claims have been amended, added or cancelled.

All of the claims were rejected in the above-referenced Office action. The rejections can be summarized as follows:

- claims 1 and 4 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 4,973,902 to Dhyanchand et al. ("the Dhyanchand et al. patent");
- claims 2, 6 – 11 and 14 were rejected under 35 U.S.C. § 103(a) as being obvious in light of the Dhyanchand et al. patent and U.S. Patent 4,347,541 to Chen et al. ("the Chen et al. patent"); and
- claims 3, 5 and 12 – 13 were rejected under 35 U.S.C. § 103(a) as being obvious in light of the Dhyanchand et al. patent, the Chen et al. patent and U.S. Patent 4,571,659 ("the Demeyer et al. patent").

In view of the following remarks, the Applicants respectfully request reconsideration and allowance of claims 1-14.

Rejections of Claims 1 and 4 Under 35 U.S.C. § 102(b)

Claims 1 and 4 are rejected under 35 U.S.C. § 102(b) as being anticipated by he Dhyanchand et al. patent. The Applicants respectfully traverse the rejections for at least the following reasons.

Claim 1 recites:

> An arc fault detector for detecting arc faults in three phase aircraft power systems, comprising:
>
> three full wave rectifiers each having an output connected to a threshold detector;
>
> a three input comparator connected to an output of each of the threshold detectors; and
>
> a fault verification circuit connected to an output of the three input comparator.

Claim 4 recites:

> The arc fault detector of claim 1, wherein the three input comparator is configured to generate a signal indicative of the outputs of any two of the threshold detectors differing by more than a predetermined amount.

Regarding claim 1, page two of the Office action states that the Dhyanchand et al. patent discloses a "three full wave rectifier means . . . for generating the signal indicative of each . . . of the three phase . . . wherein each having an output connected to a threshold detector considered to be a current sensing or sensor." (Emphasis Added).

The Applicants respectfully point out that the Dhyanchand et al. patent teaches that:

> the three phase rectifier is comprised of current source power diodes . . . [and] the diodes . . . [have] an integral current sensing lead 20'. The current in the current following lead 20' will be $1/\eta$ times the main current where η is typically on the order of 100. (Col. 2, lines 21-26).

Accordingly, the Applicants can find no such teaching in the Dhyanchand et al. patent that the current sensing or sensor is a threshold detector. Correspondingly, the Dhyanchand et al. patent does not teach "three full wave rectifiers each having an output connected to a threshold detector" as claimed in claim 1.

Page two of the Office action also states that the Dhyanchand et al. patent teaches a "three input comparator means." (Emphasis Added). The Applicants can find no such teaching in the Dhyanchand et al. patent. The Applicants respectfully point out that the Dhyanchand et al. patent teaches "A comparator 40 compares these two instantaneous signals and provides an output fault signal on lead 42. . . ." (Emphasis Added). (Col. 2, lines 63-65). Accordingly, the Applicants can only find a three-input, not two-input comparator in the Dhyanchand et al. patent. Correspondingly, the Dhyanchand et al. patent does not teach "a three input comparator connected to an output of each of the threshold detectors" as claimed in claim 1.

On pages two and three, the Office action states that the Dhyanchand et al. patent teaches a fault verification circuit "considered to be an unbalance fault detector . . . and for generating a

signal ... in response to three rectified signals from the three input comparator." First, as noted above, Applicants can find no such teaching regarding the three input comparator in the Dhyanchand et al. patent. Applicants also note that the Dhyanchand et al. patent teaches that:

> [I]t will be appreciated that the output signal of current transformer 22A will be instantaneously equal to the output of the summing junction 34 under no-fault conditions. A comparator 40 compares these two instantaneous signals and provides an output fault signal on lead 42 if there is an instantaneous imbalance in the inputs.
> (Col. 2, lines 60-66; FIG. 2).

Accordingly, the Dhyanchand et al. patent does not teach the "fault verification circuit connected to an output of the three input comparator" claimed in claim 1.

Under MPEP §2131, to anticipate a claim, the reference must teach every element of the claim. For at least the foregoing reasons, the Applicants respectfully submit that the Dhyanchand et al. patent does not teach every element of claim 1. Accordingly, claim 1 is patentable for at least these reasons. The Applicants respectfully request reconsideration and withdrawal of the rejection of claim 1.

Claim 4 depends from claim 1 and therefore includes all of the elements and limitations of claim 1. As such, claim 4 is patentable for at least the reasons provided above for claim 1 without regard to further patentable limitations contained therein. Accordingly, the Applicants respectfully request reconsideration and withdrawal of the rejection of claim 4.

Rejections of Claims 2, 6-11 and 14 Under 35 U.S.C. § 103(a)

Claims 2, 6-11 and 14 are rejected under 35 U.S.C. § 103(a) as being unpatentable the Dhyanchand et al. patent in view of the Chen et al. patent. The Applicants respectfully traverse the rejections for at least the following reasons.

Claim 2 recites:

> The arc fault detector of claim 1, wherein the threshold detectors comprise a first comparator having a first input connected to an output of one of the full wave rectifiers, a second input connected to a signal indicative of a predetermined threshold and an output.

The Office action states that:

> Dhyanchand et al. discloses all of features claimed invention except for a first input connected to an output of one of full wave rectifiers, a second input connected to a signal indicative of a predetermined threshold and an output.

First, as noted above with regard to claims 1 and 4, the Applicants can find no teachings in the Dhyanchand et al. patent of "all of features claimed invention" as indicated in the quoted section immediately above. Under MPEP § 2143.01, to establish a prima facie case of obviousness, the combined references must teach all of the claimed elements and limitations. The combination of the Dhyanchand et al. patent and the Chen et al. patent do not teach all of the claimed elements and limitations in claim 1 for the reasons provided with regard to claim 1. Because claim 2 depends from claim 1 and therefore includes all of the elements and limitations of claim 1, claim 2 is patentable for at least the reasons provided above for claim 1 without regard to further patentable limitations contained therein. Accordingly, the Applicants respectfully request reconsideration and withdrawal of the rejection of claim 2.

On pages five and six, with regard to claims 6, 8-11 and 14, the Office action states that:

> Dhyanchand et al. discloses all of features claimed invention except for means for detecting one of three rectified signals exceeds a predetermined threshold. However, Chen et al. teaches a threshold detection means (66 of figure 3 and col. 7 lines 22-46) for detecting one of three rectified a detected signal indicative of at least two of the three rectified signals differing for a time period exceeding a predetermined duration by the fault verification circuit means, wherein the detection of differences having continuously monitoring and sampling the signals indicative of the three phase.

The Office action also states that the Chen et al. patent teaches that:

> [I]t is known in the art to provide fault verification circuit means considered to be an output stage (13 of figure 1) for generating a detected signal indicative of at least two considered to be a long term delay signal, a short term delay signal, or an instantaneous trip signal of the three rectified signals differing for a time period exceeding a predetermined

> duration (col. 8 lines 19-34) wherein the detection of differences having continuously monitoring and sampling the signals indicative of the three phase (col. 7 lines 20-67). See figures 1-7.

Claim 6 recites:

An arc fault detector for detecting arc faults in three phase aircraft power systems, comprising:

means for generating a signal indicative of each of the three phases;

means for rectifying the generated signals;

means for comparing the three rectified signals; and

means for generating a signal in response to the three rectified signals differing for a time period exceeding a predetermined duration.

Claim 7 recites:

The arc fault detector of claim 6, further comprising:

means for detecting that one of the three rectified signals exceeds a predetermined threshold; and

wherein the means for generating a signal in response to the three rectified signals differing for a time period exceeding a predetermined duration generates a signal if at least one of the three filtered signals exceeds the predetermined threshold.

The Applicants respectfully point out that the Chen et al. patent teaches:

> [T]he output stage 13 provides a signal to reset all the electronic counters 83. . . . The OR gate 26 inputs includes a long term delay signal, a short term delay signal, the instantaneous trip signal and the over-temperature signal. (Col. 8, lines 19-28).

The Applicants submit that, as shown in FIG. 3, the short term delay signal 19, the long term delay signal 18 and the instantaneous trip signal 21 are each compared in each respective comparator 69, 64 and 66 and not to one another. Accordingly, the Applicants submit that the long term delay signal, the instantaneous trip signal and the short term delay signal are each

separately compared to a reference voltage and any of the three signals can send a signal to the OR gate 26 and cause the breaker to trip. The Applicants can find no teaching in the Chen et al. patent for a "means for generating a signal in response to the three rectified signals differing for a time period exceeding a predetermined duration" (Emphasis Added) as claimed in claim 6. Accordingly, the Applicants submit that the combination of the Dhyanchand et al. patent and the Chen et al. patent does not teach all of the claimed elements and limitations in claim 6. Accordingly, the Applicants respectfully request reconsideration and withdrawal of the rejection of claim 6.

Because claim 7 depends from claim 6 and therefore includes all of the elements and limitations of claim 6, claim 7 is patentable for at least the reasons provided above for claim 6 without regard to further patentable limitations contained therein. Accordingly, the Applicants respectfully requests reconsideration and withdrawal of the rejection of claim 7.

Claim 8 recites:

A method of detecting arc faults in three phase aircraft power systems, comprising:

detecting at least one of the three phases having a current exceeding a predetermined threshold;

detecting differences between the three phases; and

generating a signal indicative of differences being detected between the three phases for a time period exceeding a predetermined duration.

Claim 9 recites:

The method of claim 8, wherein the detection of differences further comprises:

generating signals indicative of each of the three phases; and

generating a signal indicative of at least two of the three signals differing by more than a predetermined amount.

Claim 10 recites:

The method of claim 9, wherein detection of differences further comprises continuously monitoring the signals indicative of the three phases.

Claim 11 recites:

The method of claim 9, wherein the detection of differences further comprises continuously sampling the signals indicative of the three phases.

Claim 14 recites:

The method of claim 8, wherein generating a signal indicative of differences being detected between the three phases for a time period exceeding a predetermined duration further comprises:

generating a signal indicative of the time period during which at least two of the three phases differ by more than a predetermined amount; and

comparing the generated signal to a signal indicative of the predetermined duration.

For the reasons related to those provided above with regard to claim 6, the Applicants can find no teaching in the Chen et al. patent for a "generating a signal indicative of differences being detected between the three phases for a time period exceeding a predetermined duration" (emphasis added) as claimed in claim 8. Accordingly, claim 8 is patentable for at least these reasons. The Applicants respectfully request reconsideration and withdrawal of the rejection of claim 8.

Because claims 9-11 and 14 depend from claim 8 and therefore include all of the elements and limitations of claim 8, claims 9-11 and 14 are patentable for at least the reasons provided above for claim 8 without regard to further patentable limitations contained therein. Accordingly, the Applicants respectfully request reconsideration and withdrawal of the rejection of claims 9-11 and 14.

Rejections of Claims 3, 5 and 12-13 Under 35 U.S.C. § 103(a)

Claims 3, 5 and 12-13 are rejected under 35 U.S.C. § 103(a) as unpatentable over the Dhyanchand et al. patent in view the Chen et al. patent as applied to claims 1-2 above, and further in view of U.S. Patent No. 4,571,659 to the Demeyer et al. patent. Applicants respectfully traverse the rejections for at least the following reasons.

On page seven, the Office action states that:

> Dhyanchand et al. in view of Chen et al. discloses all of features claimed invention except for an integrator in the threshold detector configured to integrate the output of the first comparator comparing the magnitude generated signals indicative of each of three phase to a predetermined threshold and generating a signal for each phase indicative of the magnitude of the signal relative to the threshold. However, Demeyer et al. teaches that it is known in the art to provide an integrator (12 of figures 1-56 and col. 2 lines 10-20 and 55-68) in the threshold detector (figures 6-7) configured to integrate the output of the first comparator (14 of figures 1-5) for comparing the magnitude generated signals indicative of each of three phase to a predetermined threshold and generating a signal for each phase indicative of the magnitude of the signal relative to the threshold (col. 2 lines 1-30).

While the Applicants admit having identified no such teaching in the Demeyer et al. patent, even if the Demeyer et al. patent reference were to include the above-discussed teaching, the Demeyer et al. patent does not overcome the deficiencies discussed with regard to the combination of the Dhyanchand et al. patent and the Chen et al. patent for independent claims 1, 6 and 8. Because claims 3 and 5 depend from claim 1 and therefore have all of the limitations and elements of claim 1, and claims 12-13 depend from claim 8 and therefore have all of the limitations and elements of claim 8, claims 3, 5 and 12-13 are not unpatentable over the Dhyanchand et al. patent in view of the Chen et al. patent and further in view of the Demeyer et al. patent.

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In view of the above remarks, the Applicants believe that claims 1-14 in the application are in condition for allowance, and respectfully request reconsideration and allowance of claims 1-14. If there are any questions regarding the prosecution of this application, the Examiner is invited to contact the undersigned attorney at the phone number listed below.

Respectfully submitted,
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